85. (As Filed) The device of claim 66, wherein said second plurality of contact holes are formed by a photoresist process.

86. (As Filed) The device of claim 66, wherein said second plurality of contact holes are formed by a wet etch process.

87. (As Filed) The device of claim 66, wherein said second plurality of contact holes are formed by a dry etch process.

88. (Previously Once Amended) The device of claim 66, wherein said second plurality of contact holes are filled by a CVD process.

REMARKS

Claims 1-28, 30-39, 41-43, 45-70, 72-80 and 82-88 were pending in this application. Claims 1, 5, 6, 10, 15, 20, 23, 27, 30, 31, 34, 36 and 39 have been amended. No other claims have been either amended, added or canceled. Hence, claims 1-28, 30-39, 41-43, 45-70, 72-80 and 82-88 remain pending. Reconsideration of the subject application as amended is respectfully requested.

Claims 12-28, 30-39, 41-43, 45-51, 55-56, 58, 59, 64-70, 72-76, 80, 83 and 84 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Gutierrez, U. S. Pat. No. 5,069,749.

Claims 1, 3-6, 8-11, 52-54, 60-62, 77-79 and 85-87 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Gutierrez as applied to claims 15, 41 and 64 above and further in view of Park, U. S. Pat. No. 5,318,923, taken with Erb, U. S. Pat. No. 4,707,457.

Claims 2, 7, 57,63, 82, and 88 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA, Guttierez, Park, and/or Erb as applied to claims 1, 6, 66 and 88 above, and further in view of Wolf, SILICON PROCESSING FOR THE VLSI ERA - VOLUME II, 1990, Lattice Press, page 192.

EXAMINER INTERVIEW OF DECEMBER 10, 2001

Applicant appreciates the willingness of Examiner Pert to discuss at length the outstanding rejections of Applicant's claims and to discuss basis of patentability of the claims. With Examiner Pert's input, it was tentatively agreed that, taken as a whole, the combination of elements in the claims provide patentable material.

Considering, for example, the method for filling contact holes as provided in independent claim 1, the method includes, *inter alia*, forming a plurality of contact holes of substantially equal depth, where the contact holes have a tapered upper portion. These contact holes are then entirely filled with metal, such that the metal fills the contact holes and extends slightly beyond them. Thus, the contact holes are each completely filled, yet not over-filled. Therefore, with the combination of elements as provided in claim 1, this method, *inter alia*, obviates the need for additional patterning subsequent to filling the contact holes to avoid circuit failure between metal wires.

Other elements of the method provided in claim 1 include forming an upper contact hole in a layer over the previously discussed lower contact holes. Alignment of the upper and lower contact holes is aided, in part, by the increased width of the upper portion of the lower contact holes. The upper contact holes are then filled with metal and contacted with an upper wiring layer.

Similarly, other independent claims provide limitations and/or advantages, that when taken as a whole, the combination of elements provide patentable subject matter. For example, independent claim 17 provides, *inter alia*, forming an insulating layer of substantially uniform thickness wherein contact hole is formed with a tapered upper portion and subsequently filled entirely by a conductive material. Alternatively, independent claim 23 provides, *inter alia*, a first plurality of contact holes with substantially equal depth and tapered upper portions. The contact holes are filled entirely by a conductive material.

To check the validity of the tentative agreement that, taken as a whole, the combination of elements in the claims provide patentable material, after the interview Examiner Pert performed another search for relevant prior art in addition to that provided in the previous office actions. While not setting forth a complete rejection, Examiner Pert

verbally requested that discussion of the results of the search, Fisher et al. (U.S. Patent 4,917,759), be reflected in the record. Applicant appreciates Examiner Pert's efforts in identifying additional prior art and in alerting Applicant verbally of the prior art to thus avoid an additional non-final rejection in the case.

Fisher et al. provides disclosure relative to forming self-aligned vias in multi-level integrated circuits. More particularly, Fisher et. al. forms multi-level interconnect by forming metal layers (1st aluminum [14], tungsten [15], 2nd aluminum [20], and 3rd aluminum [26]) covering the surface of the device and then patterning one of the metal layers (20) to form a via (21). Fisher et al. at Figs. 1-6. This is in direct contrast to Applicant's invention provided in claim 1 where, *inter alia*, an interconnect is formed by filling a contact hole such that the metal layer filling the contact hole extends slightly beyond the contact hole, rather than forming a metal layer from which a via will be subsequently patterned. The teachings of Fisher et al. are starkly contrasted with Applicant's invention as provided in claim 1 because, as is taught in Fisher et al., Applicant's invention as provided in claim 1 is not desirable.

Thus, not only does the disclosure of Fisher et al. contradict Applicant's claim 1, Fisher et al. teaches that the process provided by Applicant's claim 1 should not be used. More specifically, Fisher et al. teaches that the method of forming metal layers overlying the surface of a device and subsequently etching back is necessary as it is not possible to assure "alignment of upper and lower metal layers with an aperture formed in a dielectric for a via." Id. at col. 1, ll. 53-57. Fisher et al. continues to recount a number of problems associated with forming interconnect by methods other than those provided in the detailed description. Id. at col. 1, l. 63 – col. 2, l. 19. Some of the methods disparaged by Fisher et al. include forming vias by forming a contact hole in an insulating layer and filling with a metal as provided in Applicant's claim 1. Id. at col. 1, l. 63 – col. 2, l. 19.

Other methods actively discouraged by Fisher et al. include a method for aligning vias by "framing the via". Id. at col. 2, ll. 7-19. As discussed, framing the via is done by forming an additional wide metal layer on either side of the via as illustrated in Figures 1-6. Id. at col. 3, ll. 47-49. More specifically, the frame is provided by metal layer 16 and 13 under via 21 and metal layer 26 over via 21. Id. at Figure 6. Thus, provided with the disclosure of Fisher et al., one of ordinary skill in the art would be actively dissuaded from performing the

steps provided in Applicant's claim 1. With such explicit teachings away from the invention of claim 1, Fisher et al. does not motivate or suggest any combination that would render Applicant's claim obvious.

While moot in light of the interview with Examiner Pert, for completeness, each of the outstanding rejections are addressed below.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103

Claims 12-28, 30-39, 41-43, 45-51, 55-56, 58, 59, 64-70, 72-76, 80, 83 and 84 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Gutierrez, U. S. Pat. No. 5,069,749. Applicant respectfully traverses the rejection with respect to independent claim 12.

Independent claim 12 provides a method of forming a substrate with contact holes filled by multi-step deposition of conductive layers. The method includes, *inter alia*, "forming a first contact hole of substantially equal depth to other contact holes in the first insulating layer by removing a portion of the first insulating layer to expose said junction layer, *the first contact hole having a tapered upper portion*". Conductive material is formed in the via and "overgrown appropriately to prevent misalignment with a second contact hole to be formed above the first contact hole." 5,683,938 at Fig. 2B; col. 3, ll. 40-43. Thus, the first contact hole is tapered to ensure alignment between interconnect layers.

Neither Gutierrez nor the AAPA disclose, teach or suggest the tapered upper portions as provided in claim 12. Thus, Applicant agrees that "Gutierrez does not textually teach contact holes with 'tapered upper portions', or contact holes with an 'upper portion width greater than a lower portion width' as claimed by [A]pplicant". Office Action of 9/26/01 at 3. However, Applicant does not agree that "Gutierrez does clearly depict such contact holes in the cover Figure to his patent" in such a way that teaches, suggests or motivates one of ordinary skill in the art at the time of Applicant's invention to employ the method as provided in claim 12.

Rather, if anything, Figure 8 of Gutierrez teaches that the shape of the vias is irrelevant as any change in width of the various vias is simply happenstance, not an intended result. For example, vias 218 and 220 have a lower portion width roughly equal to the upper

portion width, while via 222 has a lower portion width greater than an upper portion width. Thus, rather than teach Applicant's invention provided in claim 12, such a disparity of shapes actually teaches away from Applicant's invention as provided in claim 12 by suggesting that the shape of the vias is irrelevant.

Said another way, Figure 8 of Gutierrez would not motivate, teach or suggest Applicant's claim 12 to one of ordinary skill in the art at the time of Applicant's invention. Hence, for at least the aforementioned reasons, independent claim 12, as well as those claims dependent therefrom, are in condition for allowance. Furthermore, independent claims 15, 17, 20, 23, 27, 30, 31, 32, 34, 36, 39, 64 and 66 each contain somewhat similar limitations to that provided in claim 12. Thus, each of these claims, as well as those that depend therefrom, are in condition for allowance.

Claims 1, 3-6, 8-11, 52-54, 60-62, 77-79 and 85-87 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Gutierrez as applied to claims 15, 41 and 64 above and further in view of Park, U. S. Pat. No. 5,318,923, and further in view of Erb, U.S. Pat. No. 4,707,457. Applicant respectfully traverses the rejection with respect to independent claim 1.

Independent claim 1 provides a method of forming a substrate with contact holes filled by multi-step deposition of conductive layers. The method includes, *inter alia*, filling a first metal layer into the first plurality of contact holes, the first metal layer being grown over and extending slightly beyond said first plurality of contact holes.

In contrast, Park teaches that this is not possible. More specifically, the purpose of Park is to avoid the problems associated with filling a via using a single metal layer as illustrated in Figure 1 of Park. Park at col. 1, ll. 29-48. To avoid this problem, Park first covers the inner wall of the via and the upper surface of the insulator with a metal layer (Fig. 2A) and subsequently fills the inner portion of the via with a second metal layer such that the metal does not extend slightly beyond (Fig. 2B). Thus, Park teaches away from Applicant's method as provided in claim 1 by teaching that it is not desirable to fill the via entirely with a first metal layer. As such, Park is not properly combinable with any reference to render Applicant's claim 1 obvious.

Further, Park does not teach filling the via such that the metal extends slightly beyond. Indeed, Park teaches that the via is under-filled as illustrated in Figure 2B. Thus, for this additional reason, Park does not anticipate Applicant's claim 1.

Erb is similarly flawed. For example, among other inadequacies, Erb fails to disclose, teach or suggest filling a first metal layer into a via such that it extends slightly beyond the via.

Both because the combination of references is not proper and because the combination fails to teach every limitation of claim 1, the combination does not render claim 1 obvious. Hence, claim 1, as well as those dependent therefrom, are in condition for allowance. Furthermore, independent claims 5, 6 and 10 include, among others, limitations similar to the previously described. Accordingly, independent claims 5, 6 and 10, as well as those dependent therefrom, are also in condition for allowance.

Claims 2, 7, 57,63, 82, and 88 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA, Guttierez, Park, and/or Erb as applied to claims 1, 6, 66 and 88 above, and further in view of Wolf, SILICON PROCESSING FOR THE VLSI ERA - VOLUME II, 1990, Lattice Press, page 192. At least because each of the aforementioned claims properly depend from allowable independent claims, they are also in condition for allowance.

In sum, for at least the aforementioned reasons, claims 1-28, 30-39, 41-43, 45-70, 72-80 and 82-88 are all in condition for allowance and such is respectfully requested. Of note, claims 1, 5, 6, 10, 15, 20, 23, 27, 30, 31, 34, 36, 39 and 41 have been amended to correct typographical and/or grammatical errors. The amendments do not change the scope of the claimed subject matter.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

PATENT

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Once Amended Herein) A method for filling contact holes with metal by two-step deposition of metal layers, said method comprising the steps of:

providing a silicon substrate;

forming a field oxide layer and a junction layer and gate electrode on said silicon substrate;

forming a first insulating layer on exposed portions of the field oxide layer, the junction layer, and the gate electrode;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively the first plurality of contact holes having a tapered upper portion;

filling a first metal layer into the first plurality of contact holes, entirely, the first metal layer being grown over and extending slightly beyond said first plurality of contact holes [hoes];

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively and

filling a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern respectively.

2. (As Filed) A method according to claim 1, wherein the first metal layer and subsequently the second metal layer are formed by chemical vapor deposition method.

3. (Previously Once Amended) A method according to claim 1, wherein the filling a second metal layer fills the second plurality of contact holes to a substantially equal depth.

4. (As Filed) A method according to claim 1, wherein the first and second metal layers are selective tungsten layers, respectively, and the first and second plurality of contact holes are filled with the first and second metal layers of the selected tungsten layers, respectively.

5. (Once Amended Herein) A method for filling contact holes with metal by a two-step deposition of metal layers, said method comprising the steps of:

providing a silicon substrate;

forming a field oxide layer and a junction layer and gate electrode on said silicon substrate;

forming a first insulating layer on exposed portions of the field oxide layer, the junction layer, and the gate electrode;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively the first plurality of contact holes having a tapered upper portion;

filling a first metal layer into entire first plurality of contact holes by one single step, the first metal layer being grown over and extending slightly beyond said first plurality of contact holes;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively and

filling a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern respectively.

6. (Once Amended herein) A method of forming a substrate with contact holes, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the gate electrode;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively, the first plurality of contact holes having a tapered upper portion;

forming a first conductive material layer into the first plurality of contact holes, entirely, the first conductive material layer being grown over and extending slightly beyond said first plurality of contact holes;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern, respectively; and

forming a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern, respectively.

7. (Previously Once Amended) A method according to claim 6, wherein the first conductive material layer and subsequently the second conductive material layer are formed by a chemical vapor deposition process.

8. (Previously Once Amended) A method according to claim 6, wherein the forming a second conductive material layer fills the second plurality of contact holes to a substantially equal depth.

9. (Previously Once Amended) A method according to claim 6, wherein the first and second conductive material layers comprise first and second tungsten layers, respectively, and the first and second plurality of contact holes are filled with the first and second tungsten layers, respectively.

10. (Once Amended Herein) A method of forming a substrate with contact holes, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the gate electrode;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively, the first plurality of contact holes having a tapered upper portion;

forming a first conductive material layer into entire first plurality of contact holes in a continuous step, the first conductive material layer being grown over and extending slightly beyond said first plurality of contact holes;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern, respectively; and

forming a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern, respectively.

11. (As Filed) A method according to claim 10, wherein said steps of forming said first and said second conductive material layers comprise filling said first and said second plurality of contact holes, respectively.

12. (Previously Twice Amended) A method of forming a substrate with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a substrate;

forming an oxide layer and a junction layer on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the junction layer;

forming a first contact hole of substantially equal depth to other contact holes in the first insulating layer by removing a portion of the first insulating layer to expose said junction layer, the first contact hole having a tapered upper portion;

forming a first conductive material layer into the first contact hole, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first contact hole;

forming a second contact hole by removing portions of said second insulating layer to expose the first conductive material layer; and

forming a second conductive material layer into said second contact hole to contact the first conductive material layer.

13. (As Filed) A method as in claim 12, further comprising:

forming a third contact hole by removing portions of the second insulating layer to expose the conductive layer pattern; and

forming the second conductive material layer into the third contact hole to contact the conductive layer pattern.

14. (As Filed) A method as in claim 12, wherein said first and said second conductive material layers comprise a metal.

15. (Twice Amended Herein) A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a silicon substrate;

forming an oxide layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the gate electrode;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said gate electrode, the first plurality of contact holes having a tapered upper portion;

filling a first conductive material layer into the first plurality of contact holes, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern; and

filling a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern.

16. (As Filed) A method as in claim 15, wherein said first and second conductive material layers comprise first and second metal layers.

17. (Previously Once Amended) A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive material layers, said method comprising:

providing a substrate;

forming an oxide layer and a first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the first conductive layer pattern, wherein a thickness of the first insulating layer is substantially uniform;

forming a first contact hole by removing a portion of the first insulating layer to expose said first conductive layer pattern, the first contact hole having a tapered upper portion;

forming a first conductive material layer into the first contact hole, filling said first contact hole entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first conductive material layer;

forming second and third contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the second conductive layer pattern, respectively; and

forming a second conductive material layer into said second and third contact holes to contact the first conductive material layer and the second conductive layer pattern, respectively.

18. (As Filed) A method as in claim 17, wherein said first conductive layer pattern comprises a gate electrode.

19. (As Filed) A method as in claim 17, wherein said first and second conductive material layers comprise first and second metal layers.

20. (Once Amended Herein) A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the first conductive layer pattern;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said first conductive layer pattern, respectively, the first plurality of contact holes having a tapered upper portion;

filling a first conductive material layer into the first plurality of contact holes, entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the second conductive layer pattern, respectively; and

filling a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the second conductive layer pattern, respectively.

21. (As Filed) A method as in claim 20, wherein said first and second conductive material layers comprise first and second metal layers.

22. (As Filed) A method as in claim 20, wherein said first conductive layer pattern comprises a gate electrode.

23. (Once Amended Herein) A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a substrate;

forming an oxide layer, and first and second regions on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and said first and said second regions;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said first and second regions, the first plurality of contact holes having a tapered upper portion;

forming a first conductive material layer into, and filling entirely, the first plurality of contact holes;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first conductive material layer;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern; and

forming a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern.

24. (As Filed) A method as in claim 23, wherein said first region comprises a junction layer.

25. (As Filed) A method as in claim 23, wherein said second region comprises a gate electrode.

26. (As Filed) A method as in claim 23, wherein said first and second conductive material layers comprise first and second metal layers.

27. (Twice Amended Herein) A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the gate electrode;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively, wherein said first plurality of contact holes have an upper portion width and a lower portion width, said upper portion width greater than said lower portion width;

forming a first conductive material layer into the first plurality of contact holes, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern; and

forming a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern.

28. (As Filed) A method as in claim 27, wherein said first and second conductive material layers comprise first and second metal layers.

30. (Once Amended Herein) A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer and a junction layer on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the junction layer;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer, the first plurality of contact holes having a tapered upper portion;

forming a first metal layer into the first plurality of contact holes, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively; and

forming a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

31. (Once Amended Herein) A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the gate electrode;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said gate electrode, the first plurality of contact holes having a tapered upper portion;

filling a first metal layer into the first plurality of contact holes, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively; and

filling a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

32. (Previously Once Amended) A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer and a first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the first conductive layer pattern, wherein a thickness of the first insulating layer is substantially uniform;

forming a first contact hole by removing a portion of the first insulating layer to expose said first conductive layer pattern, the first contact hole having a tapered upper portion;

forming a first metal layer into the first plurality of contact hole, entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first contact hole;

forming second and third contact holes of substantially equal depth by removing portions of said second insulating layer to expose the first metal layer and the second conductive layer pattern, respectively; and

forming a second metal layer into said second and third contact holes to contact the first metal layer and the second conductive layer pattern, respectively.

33. (As Filed) A method as in claim 32, wherein said first conductive layer pattern comprises a gate electrode.

34. (Once Amended Herein) A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer and a junction layer and first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the first conductive layer pattern;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said first conductive layer pattern, respectively, the first plurality of contact holes having a tapered upper portion;

forming a first metal layer into the first plurality of contact holes, entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the second conductive layer pattern, respectively; and

forming a second metal layer into said second plurality of contact holes to contact the first metal layer and the second conductive layer pattern, respectively.

35. (As Filed) A method as in claim 34, wherein said first conductive layer pattern comprises a gate electrode.

36. (Once Amended Herein) A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer, and first and second regions on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the first region and the second region;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said first and said second region, respectively, the first plurality of contact holes having a tapered upper portion;

forming a first metal layer into the first plurality of contact holes, to fill said first plurality of contact holes entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively; and

forming a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

37. (As Filed) A method as in claim 36, wherein said first region comprises a junction layer.

38. (As Filed) A method as in claim 36, wherein said second region comprises a gate electrode.

39. (Twice Amended Herein) A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the gate electrode;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively, wherein said first plurality of contact holes have a tapered upper portion;

forming a first metal layer into the first plurality of contact holes, to fill said first plurality of contact holes entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively; and

forming a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

41. (Previously Twice Amended) A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive material layers, said method comprising:

providing a substrate;

forming an oxide layer and a first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the first conductive layer pattern, wherein a thickness of the first insulating layer is substantially uniform;

forming a first contact hole by removing portions of the first insulating layer to expose said first conductive layer pattern, wherein said first contact hole has an upper portion width and a lower portion width, said upper portion width greater than said lower portion width;

forming a first conductive material layer into the first contact hole, entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first contact hole;

forming second and third contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the second conductive layer pattern, respectively; and

forming a second conductive material layer into said second and said third contact holes to contact the first conductive material layer and the second conductive layer pattern, respectively.

42. (As Filed) The method of claim 41, wherein said first conductive material layer comprises a metal.

43. (As Filed) The method of claim 42, wherein said metal comprises tungsten.

45. (As Filed) The method of claim 41, wherein said first conductive layer pattern comprises a gate electrode.

46. (As Filed) The method of claim 41, wherein said first conductive layer pattern comprises a gate electrode overlying a gate oxide.

47. (Previously Once Amended) The method of claim 41, wherein said forming an oxide layer and a first conductive layer pattern further comprises forming a junction layer.

48. (As Filed) The method of claim 41, wherein said junction layer comprises a N+ junction.

49. (As Filed) The method of claim 41, wherein said junction layer comprises a P+ junction.

50. (As Filed) The method of claim 41, wherein said first conductive layer pattern comprises polysilicon.

51. (As Filed) The method of claim 41, wherein said first insulating layer comprises a first oxide layer.

52. (As Filed) The method of claim 41, wherein said step of forming said first contact hole comprises a photoresist process.

53. (As Filed) The method of claim 41, wherein said step of forming said first contact hole comprises a wet etch process.

54. (As Filed) The method of claim 41, wherein said step of forming said first contact hole comprises a dry etch process.

55. (As Filed) The method of claim 47, wherein said step of forming said first contact hole further exposes said junction layer.

56. (As Filed) The method of claim 41, wherein said first contact hole has a tapered upper portion.

57. (As Filed) The method of claim 41, wherein said step of forming said first conductive material layer comprises a CVD process.

58. (As Filed) The method of claim 41, wherein said second conductive layer pattern comprises polysilicon.

59. (As Filed) The method of claim 41, wherein said second insulating layer comprises a second oxide layer.

60. (As Filed) The method of claim 41, wherein said step of forming said second and said third contact holes comprises a photoresist process.

61. (As Filed) The method of claim 41, wherein said step of forming said second and said third contact holes comprises a wet etch process.

62. (As Filed) The method of claim 41, wherein said step of forming said second and said third contact holes comprises a dry etch process.

63. (As Filed) The method of claim 41, wherein said step of forming said second conductive material layer comprises a CVD process.

64. (As Filed) A semiconductor device comprising:

a semiconductor substrate having an oxide layer, a junction layer and a gate electrode;

a first insulating layer overlying portions of said oxide layer, said junction layer and said gate electrode, said first insulating layer having a first plurality of contact holes of substantially equal depth over said junction layer and said gate electrode, said first plurality of contact holes having a tapered upper portion;

a first metal layer filling said first plurality of contact holes so that said first metal layer is in contact with said junction layer and said gate electrode;

a conductive layer pattern on said first insulating layer spaced apart from said first metal layer;

a second insulating layer overlying portions of said conductive layer pattern, said first insulating layer and said first plurality of contact holes, said second insulating layer having a second plurality of contact holes of substantially equal depth over said first metal layer and said conductive layer pattern; and

a second metal layer filling said second plurality of contact holes, said second metal layer in contact with said first metal layer and said conductive layer pattern.

65. (As Filed) A semiconductor device comprising:

a semiconductor substrate having an oxide layer, a junction layer and a gate electrode;

a first insulating layer overlying portions of said oxide layer, said junction layer and said gate electrode, said first insulating layer having a first plurality of contact holes of substantially equal depth over said junction layer and said gate electrode, said first plurality of contact holes having a tapered upper portion;

a first conductive material layer filling said first plurality of contact holes so that said first conductive material layer is in contact with said junction layer and said gate electrode;

a conductive layer pattern on said first insulating layer spaced apart from said first conductive material layer;

a second insulating layer overlying portions of said conductive layer pattern, said first insulating layer and said first plurality of contact holes, said second insulating layer having a second plurality of contact holes of substantially equal depth over said first conductive material layer and said conductive layer pattern; and

a second conductive material layer filling said second plurality of contact holes, said second conductive material layer in contact with said first conductive material layer and said conductive layer pattern.

66. (Previously Once Amended) A semiconductor device comprising:

a semiconductor substrate having an oxide layer and a first conductive layer pattern;

a first insulating layer overlying portions of said oxide layer and said first conductive layer pattern, said first insulating layer having a first plurality of contact holes of substantially equal depth over said first conductive layer pattern, wherein said first plurality of contact holes have a tapered upper portion;

a first conductive material layer filling said first plurality of contact holes so that said first conductive material layer is in contact with said first conductive layer pattern;

a second conductive layer pattern on said first insulating layer spaced apart from said first conductive material layer;

a second insulating layer overlying portions of said second conductive layer pattern, said first insulating layer and said first plurality of contact holes, said second insulating layer having a second plurality of contact holes of substantially equal depth over said first conductive material layer and said second conductive layer pattern; and

a second conductive material layer filling said second plurality of contact holes, said second conductive material layer in contact with said first conductive material layer and said second conductive layer pattern.

67. (As Filed) The device of claim 66, wherein said conductive material layers comprise a metal.

68. (As Filed) The device of claim 67, wherein said metal comprises tungsten.

69. (As Filed) The device of claim 66, wherein said first conductive layer pattern comprises a gate electrode.

70. (As Filed) The device of claim 66, wherein said first conductive layer pattern comprises a gate electrode overlying a gate oxide.

72. (As Filed) The device of claim 66, further comprising a junction layer on said substrate.

73. (As Filed) The device of claim 72, wherein said junction layer comprises a N+ junction layer.

74. (As Filed) The device of claim 72, wherein said junction layer comprises a P+ junction layer.

75. (As Filed) The device of claim 66, wherein said first conductive layer pattern comprises polysilicon.

76. (As Filed) The device of claim 66, wherein said first insulating layer comprises a first oxide layer.

77. (As Filed) The device of claim 66, wherein said first plurality of contact holes are formed by a photoresist process.

78. (As Filed) The device of claim 66, wherein said first plurality of contact holes are formed by a wet etch process.

79. (As Filed) The device of claim 66, wherein said first plurality of contact holes are formed by a dry etch process.

80. (As Filed) The device of claim 72, wherein said first plurality of contact holes expose said junction layer.

82. (Previously Once Amended) The device of claim 66, wherein said first plurality of contact holes are filled by a CVD process.

83. (As Filed) The device of claim 66, wherein said second conductive layer pattern comprises polysilicon.

84. (As Filed) The device of claim 66, wherein said second insulating layer comprises a second oxide layer.

85. (As Filed) The device of claim 66, wherein said second plurality of contact holes are formed by a photoresist process.

86. (As Filed) The device of claim 66, wherein said second plurality of contact holes are formed by a wet etch process.

87. (As Filed) The device of claim 66, wherein said second plurality of contact holes are formed by a dry etch process.

88. (Previously Once Amended) The device of claim 66, wherein said second plurality of contact holes are filled by a CVD process.